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DEVELOPMENT OF A DLLRF USING COMERCIAL UTCA PLATFORM

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Abstract

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Abstract

The Digital LLRF of ALBA has been implemented using commercial cPCI boards with WXP Drivers, Virtex-4 FPGA, fast ADCs and fast DACs. The firmware of the FPGA is based on IQ demodulation technique and the main feedback loops adjust the phase and amplitude of the cavity voltage and also the resonance frequency of the cavity. But the evolution of the market is moving towards uTCA technology and due to the interest of this technology by several labs, we have developed at ALBA a DLLRF using a HW platform based on uTCA commercial boards and Virtex6 FPGA. The paper will present the development done and will compare it with respect the cPCI one.

INTRODUCTION

ALBA is a 3GeV synchrotron light source located in Barcelona and operating with users since May 2012. The 500MHz RF system of the SR is composed of six cavities, each one powered by combining the power of two 80 kW IOTs CW through a Cavity Combiner (CaCo).

The Digital LLRF of ALBA was developed in 2006 using commercial cPCI boards from Nutaq with Virtex-4 FPGA, fast ADCs, fast DACs and a Windows XP CPU as host PC. The main advantage of using commercial platforms is the reduction of HW development and integration costs, since commercial products usually provide drivers for different operating system and an FPGA project frame or skeleton where the user can merge their algorithms or digital signal processing. This offers the possibility to developed tailored control algorithms to the specific needs of the user/accelerator when reduced or limited manpower is available.

In the ALBA case the main loops implemented in this board were meant to control the amplitude and phase of the cavity voltage within 0.1% rms amplitude resolution and 0.1° rms phase resolution using the very well-known IQ demodulation technique [1]. A resonant loop was also implemented to keep constant the diphase between the forward power of the cavity and the cavity voltage by moving a plunger inwards and outwards the cavity body.

The large processing capabilities and flexibility of the FPGAs allowed us implementing low-cost updates of the system over the last years that improved usability and reliability of the RF systems. Some of these extra-utilities developed in the LLRF are automatic conditioning, automatic start-up of RF systems, automatic recovery of cavities with circulating beam, feed-forward loops for RF Trip compensation (phase and amplitude modulation), beam loading compensation [2] and fast data logger for post-mortem analysis. However, this cPCI FPGA board is only available with Windows XP drivers and thus not suitable for new developments. For this reason and taking also into account that industry is continuously offering more powerful FPGAs with higher processing capabilities at lower costs, we decided to implement a digital LLRF based on a different HW platform for new DLLRF collaboration projects established with Diamond Light Source, UK, and Sirius Light Source, Brazil. [3, 4]

NEW HW PLATFORM FOR ALBA LLRF

uTCA

Flexibility, performance and cost were the keys aspects when selecting the new HW standard for ALBA LLRF. The uTCA is an open standard for building performance switched fabric computer systems in a small form factor developed by PICMG and with more than 100 companies participating in it. It offers high levels of modularity and configurability through the use of Advanced Mezzanine Cards (AMC) [5]. These are daughter boards that can offer extra HW capabilities to your system in terms of ADCs, DACs, communication ports and other utilities. The uTCA also provides point-to-point, dual and mesh topologies for Ethernet, Fibre Channel, PCI Express and Serial RapdiIO channel up to a total bandwidth of 2.5Tbps. Presently, there are hundreds of different AMC's and uTCA carriers available.

AMC Perseus 6010 from Nutaq

As shown in Figure 1, the Perseus 6010 from Nutaq is a mid-size AMC for UTCA platform with a Virtex-6 FPGA and a high-pin-count FMC expansion site that allows double stacking FMC boards: the MI125 with 16ADC-14bits and the MO1000 with 8DACs – 14bits. It supports multiple switch fabrics (PCIe, GigE, SRIO) and software development tools for FPGA programming [6]. It also offers a high density connector, the mestor interface, where an expansion board with 32 configurable digital input/outputs can be connected.

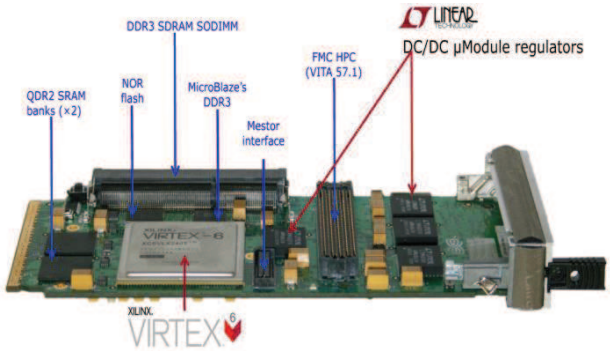

Figure 1: Main HW components of Perseus 6010 Board.

This board was selected because the already mentioned advantages of the uTCA standard and because it had been considered that offers the best cost ratio per ADC-DAC channel. The double stacking FMC option allowed connecting 16ADCs-14bits-125MHz and 8DACs-14bits-

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1GHz in a single FMC connector, resulting in a very compact solution.

On the other hand, the higher processing capabilities of the Virtex-6 FPGA uTCA platform compared to the Virtex-4 cPCI platform allowed us integrating the equivalent signal processing of two LLRF systems into a single Perseus Board, reducing considerably the series production costs.

Table 1 shows the comparison of the main features between the cPCI and uTCA platforms used in ALBA DLLRF.

Table 1: Comparison of ALBA LLRF HW Platforms

Feature	cPCI	uTCA
FPGA Type	Virtex-4	Virtex-6
FPGA Occupied Slices	91%	30%
# Controlled cavities	1	2
# ADCs & DACs	8ADCs 8DACs	16ADCs 8DACs
Cost	20,000 €	22,000 €
OS Drivers	WXP	Linux

GENERAL LLRF CHARACTERISTICS

The ALBA uTCA LLRF was developed to provide up to 4 RF Drives and to be able to control up to 2 cavities depending on the configuration selected by the user, which are:

- Conf 1: Control of one multi-cell cavity (5 or 7 cells) with one RF drive and two plungers for resonance and field flatness tuning
- Conf 2: Control of up to two normal conducting single cell cavities driven by two amplifiers each (4 RF Drives)
- Conf 3: Control of one Super Conducting Cavity driven by up to four independent RF Drives (4 RF Drives)

In overall up to 16 RF signals can be monitored and controlled by the LLRF. A down-conversion front end was assembled to transform these RF signals from 500MHz to 20MHz-IF signals. The IF signals are later sampled at 80MHz by the ADCs of the Perseus Board to perform an IQ Digital Demodulation. The FPGA applies the control loops/DSP algorithms to these signals to compute the 20MHz-IF control signals to be sent to the DACs of the system. These IF-Control Signals are also up-converted to RF in the front End and sent to pin diode switches controlled by the Perseus Board. In case an interlock is detected, like high reverse power of the cavity, these pin diode switches are opened.

Figure 2 depicts the main HW components of the uTCA LLRF System and its interfaces with RF signals.

The Digital I/Os of the Perseus mestor connector are used to interface other subsystems of the RF plant like motor controllers of the plungers, vacuum controllers, PLC or slow interlocks systems, pin diode switches and others.

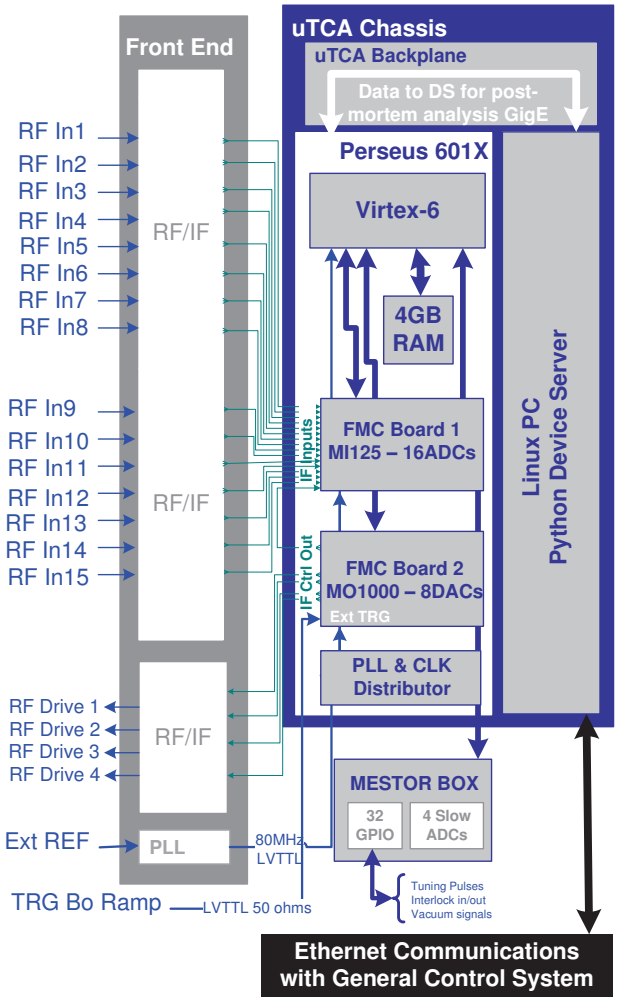

Figure 2: LLRF HW.

LLRF CONTROL: IQ VS POLAR LOOPS

The main control loops implemented in the cPCI ALBA LLRF were based on IQ demodulation. The main advantages of IQ Loops compared to Polar loops are simplicity of the IQ demodulation (use of low FPGA resources), smaller group delay and the possibility of using the same PID Loop for both IQ components. On the other hand, the main advantage of the Polar Loops compared to the rectangular loops is that amplitude and phase loops can be enabled and adjusted independently, establishing different loop bandwidths for the phase loop and for the amplitude loop if needed.

In the ALBA case, the bandwidth of the IQ loops was set to 1 kHz, ten times lower than the frequency tune (around 10 kHz). Higher bandwidths are easily achievable, but if operating with beam, the synchrotron tune is excited and the beam blows up.

The switching frequency of the ALBA RF amplifiers HVPS is below 1 kHz, so this BW was enough for operation. However, lower values of synchrotron tunes like in Max-IV (~1 kHz) or Sirius (~2 kHz) can make this approach unfeasible. For this reason a new feed-back loop strategy based both in polar and rectangular loops has been implemented in the uTCA ALBA LLRF.

Slow and Fast IQ Loops Strategy

In order not to interfere with the synchrotron tune of the beam, the bandwidth range of the IQ Loops controlling the cavity voltage was set between [0.1, 1000] Hz, using a PI with an accumulator of 40 bits. This loop has been called the "slow IQ Loop". Obviously, this BW is not able to cope with the switching frequency ripples induced by RF amplifiers PS. To overcome this problem, a second IQ loop with an adjustable bandwidth of [1, 50] kHz was implemented using a PI with 32 bits accumulator. This loop is meant to be applied only on the output of the amplifier. For doing so, the FPGA removes the average component (80Hz low pass filter) of the amplifier output signal obtaining in this way the high frequency noise component induced by the amplifier PS. This noise signal is then sent to the "Fast IQ" loop and the calculated control signal is added to the control outputs of the "slow IQ". The result of both loops working simultaneously ensures a constant phase and amplitude of the cavity voltage without exciting the synchrotron frequency at the same time that we ensure the removal of the high frequency ripples of the RF amplifiers before those reach the cavity

Polar Loops Strategy

Similarly to the Slow and Fast IQ loops, a PI loop with an adjustable bandwidth between [0.1, 1000] Hz was programmed to control the amplitude of the cavity voltage (PI accumulator of 40 bits). For doing so, the Cordic Algorithm was used to translate the IQ components of the controlled signal into Amplitude and Phase. This translation takes 16 FPGA clocks. On the other hand, a PI loop with an adjustable bandwidth of [1, 50] kHz (PI accumulator 32 bits) has been implemented to control the phase of the Forward Power of the Cavity, also provided by the Cordic algorithm. The amplitude computed by the amplitude loop and the phase provided by the phase loop are translated to IQ again through cordic algorithm (16 FPGA extra clocks). These loops keep the phase of the Cavity Forward Power constant and the tuning or resonance loop compensates the phase disturbances of the Cavity Voltage induced by the beam loading effect.

IQ vs Polar: Performance Comparison

The Polar and IQ loops have the same type of PI accumulators which should provide similar bandwidth measurements. However, the group delay of the Polar loops is 32 clocks longer respect to the IQ loops. In order to measure the effect of this longer group delay, a test setup was implemented with a voltage control attenuator placed between the RF Drive of the LLRF and the LLRF input (cavity voltage). With this setup the Polar Amp loop performance was compared to the Slow IQ performance. As observed in Figure 3, the bandwidth when using low Ki values (below 1000) is similar for both cases, but when increasing Ki values the Slow IQ Loops is capable to reach 30kHz bandwidth, while the amplitude loop becomes unstable when 25kHz perturbations are applied.

When combining Fast+Slow IQ loops or Amp&Ph Loops the achieved bandwidth is much better as shown in Figure 4. In this case, both approaches are capable to reach easily 50 kHz bandwidth, although the IQ loops still are capable of higher sideband attenuations.

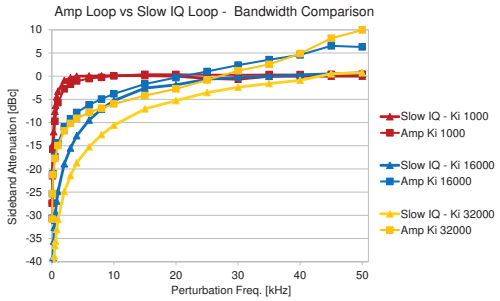

Figure 3: Amp vs Slow IQ loops – BW Comparison.

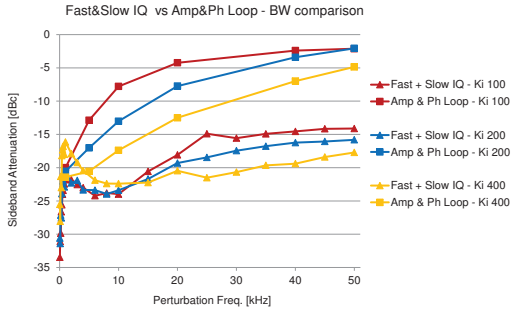

Figure 4: Amp&Ph vs Slow&Fast IQ – BW Comparison.

CONCLUSIONS

A new DLLRF based on a commercial uTCA platform has been developed in ALBA with the same utilities than the previous cPCI platform plus new features that make this system capable to control three different kinds of cavities: Booster multi-cell cavity, single-cell HOM normal conducting cavity and super conducting cavities.

Thanks to the processing power of new FPGAs, Polar and rectangular loops were implemented in this system and their performance was compared. At low frequencies the performance is similar and depending on the machine requirements, the loops can be tailored to the required bandwidth imposed by the disturbances of the RF systems.

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