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DIGITAL LLRF FOR MAX-IV

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Abstract

The MAX IV facility consists of a 3 GeV Storage Ring (SR), a 1.5 GeV SR, and a linear accelerator (fed by two guns) that serves as a full-energy injector to the rings, but also as a driver for the Short Pulse Facility. The RF systems of the two SRs work at 100MHz. There are 6 normal conducting capacity loaded accelerating cavities and three Landau passive cavities in the 3GeV SR. In the 1.5GeV SR there are two accelerating cavities and two Landau cavities with the same characteristics. Each of these cavities is fed by a modular 60kW SSA. In the 3 GeV SR the power will be doubled by adding a second SSA when required.
A digital Low Level RF system has been developed using commercial uTCA boards, with a Virtex-6 FPGA mother board (Perseus 601X) and two double stack FMC boards with fast ADCs and DACs. The large capabilities of state-of-the-art FPGAs allowed including the control of two normal conducing cavities and two landau cavities in one single LLRF system, reducing the development costs. Other utilities like the handling of fast interlocks and post-mortem analysis were also added to this system. This paper summarizes the main capabilities and performance of this DLLRF.

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INTRODUCTION

The MAX IV 3 GeV machine [1] is the first ultralow emittance storage ring based on the multibend lattice, which is currently being commissioned in Lund, Sweden.

The main parameters are presented in Table 1.

Table 1: MAX IV 3 GeV Ring Parameters [2]

Energy	3	GeV
Max Current	500	mA
Circumferences	528	m
RF- Frequency	99.931	MHz
Main Cavity Voltage	1.02	MV
Energy Loss per turn w/o IDs	360	keV
Synchrotron Frequency	[0.9 – 1.17]	kHz

The RF systems of the 3GeV ring are composed of 6 normal conducting capacitive load cavities working at 100MHz that are presently fed by one 60kW SSA amplifier and that will be fed by the combined power of two 60kW SSA amplifiers when the final design SR current is achieved and all the Insertion Devices of the SR are installed. There are also 3 third harmonic passive capacitive-loaded cavities in the 3GeV SR.

A digital LLRF system has been implemented using commercial uTCA boards and based on the ALBA DLLRF [3].

In order to reduce production costs and taking advantage of the high processing resources and powerfulness of new FPGA families, the control of two independent cavities was integrated into a single LLRF system. Also thanks to the modularity of uTCA systems a second FPGA board was added to this system for ancillary utilities like Fast Interlocks handling and Landau Tuning.

The LLRF system was assembled in 2012 and successfully commissioned with beam in 2013. The main utilities and HW components of this system will be explained in next points.

MAX-IV DLLRF HW

The main HW components of Max-IV DLLRF are:

- Digital HW: uTCA FPGA mother board + FMC boards for ADCs and DACs
- Front Ends for RF Drives upconversion
- Local Timing for LO generation and FPGA clock synchronization with MO reference

Figure 1shows a layout of the main HW components of the DLLRF and its signals interactions.

Digital Hardware: Perseus 601X

The main Digital HW of the Max-IV LLRF is a commercial uTCA board, the Perseus 6010 from Nutaq. This board has a Virtex-6 FPGA, a FMC slot and mestor expansion bus that provides 32 GPIO bus and 4 slow ADCs.

Nutaq also offers FMC modules with ADCs and DACs that can be double stack and thus, connected in pairs into a single FMC slot. The FMC boards used for the Max-IV LLRF were the MI125 FMC board with 16 ADCs – 14 bits – 125MHz and the MO1000 FMC Board with 8DACs – 14 bits – 1000MS.

As shown in Figure 1, the DLLRF of Max-IV is composed of two FPGA Perseus boards: The Loops Board with 16 high BW ADCS and 8 DACs (FMC MI125 and FMC MO1000) and the Extra Diagnostics board with only 16 high BW ADCs (FMC MI125).

The Loops Board processes the RF signals involved in the main feed-back loops like cavity voltage, forward power, MO and others, while the Diagnostics Board processes mainly the interlock signals like reverse power at different points of the RF plants.

Both boards interchange information from/to the Host PC through the uTCA backplane.

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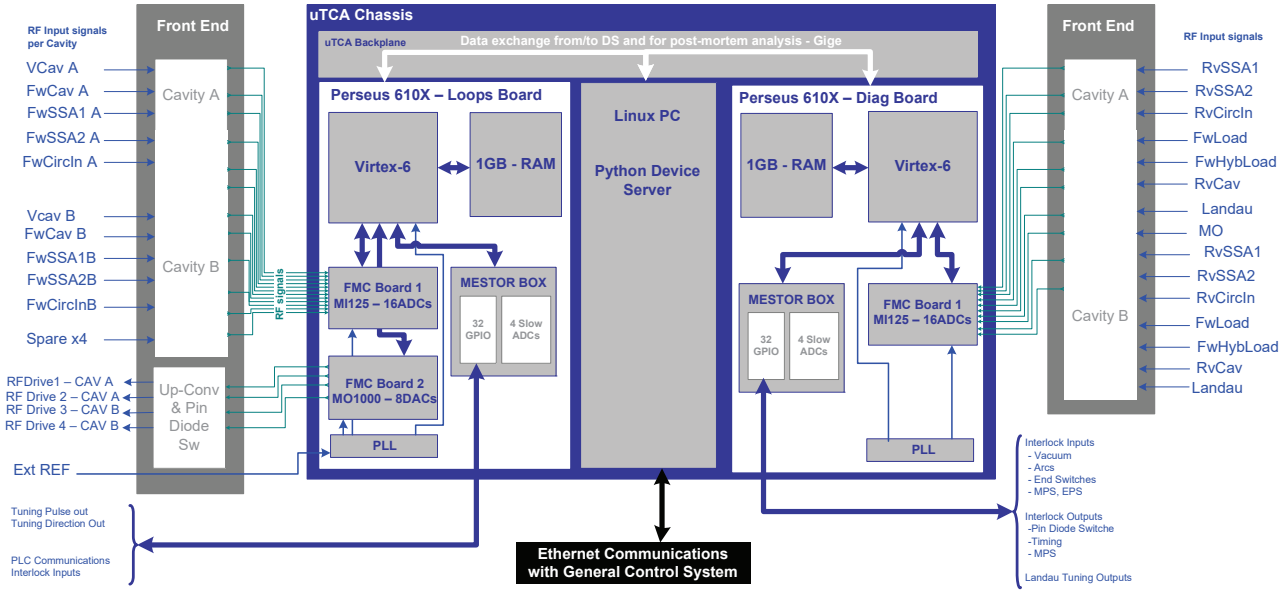

Figure 1: DLLRF HW Scheme for Max-IV.

Front Ends

Since the RF Frequency of Max-IV is around 100MHz and the ADCs BW of the FMC MI125 is 200MHz, the RF signals are directly sampled at 80MHz. The Front Ends are used simply to provide BNC test points of the main RF signals for monitoring purposes through the use of directional couplers. Direct RF sampling avoids the use of analogue components reducing the distortion that may be induced by them (non-linear response, saturation, attenuation, LO leakage and others) and increases the reliability by reducing number of components.

The Front Ends are also used to up-convert the IF-20MHz control signals provided by the DACs of the Perseus boards to 100MHz. To perform this up-conversion, the MO signal is mixed with a 20MHz signal to generate a 80MHz Local Oscillator signal

The up-converted RF Drives are sent also to pin diode switches controlled by the Diagnostics Board. These switches are opened in less than 1us if a reverse power or other interlocks are detected.

Timing

Since the RF signals are directly sampled by the ADCs, the FPGA clock must be synchronized and locked with the MO. For doing that, a PLL from Texas Instruments (CDC7005-EVM) with a VCXO working at 80MHz is used. The reference signal to lock this PLL is the MO signal itself. This PLL board also provides a clock fan-out and a frequency divider that is used to provide the 20MHz IF required for the generation of the 80MHz-LO signal.

MAX-IV DLLRF FW

IQ Digital Demodulation

All 100MHz - RF signals are sampled by the ADCs of the Perseus boards at 80MHz, providing a sample every 1.25 periods of the RF Input. The sampled signals are demultiplexed and signed inverted when required to perform an IQ Digital Demodulation. These outputs are also sent to a multiplexer so the user can select which RF signals will be controlled. In normal operation, the selected signal will be the cavity voltage, although in some cases like during the conditioning of the cavity, other signals like the Forward Power of the Cavity or the Output of the Amplifier may be more convenient to control.

PI Loops for Voltage Control: IQ vs Polar

Taking advantage of the large processing resources of the Virtex-6 FPGA families, two loop strategies were implemented in the Max-IV LLRF: Polar loops (amplitude and phase) and Rectangular or IQ loops.

The main advantages of IQ Loops compared to Polar loops are smaller group delay and the possibility of using the same PI Loop for both IQ components. The main advantage of the Polar Loops compared to the rectangular loops is that amplitude and phase loops can be enabled/adjusted independently, establishing different loop bandwidths for the phase loop and for the amplitude loop if needed.[4]

Figure 2 and Figure 3 show the long term stability of LLRF amplitude and phase loops tested at high power in Max-IV. The polar and rectangular loops show very similar stability values. Table 2 summarizes these values.

Table 2: Max-IV LLRF Loops Stability

Amplitude error	0.02% peak to peak
Phase Error	0.01º peak to peak

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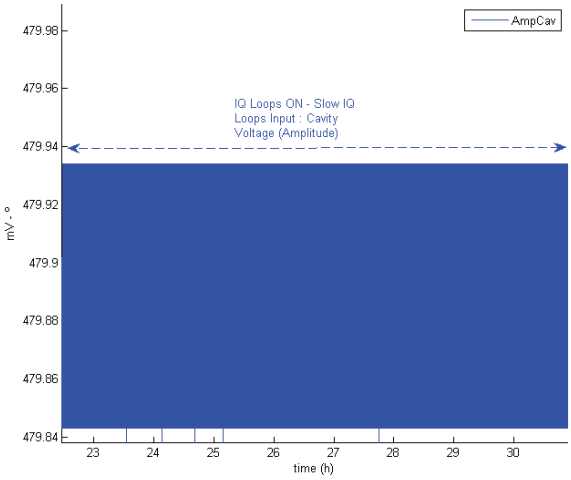

Figure 2: Long term stability of Amplitude Loop.

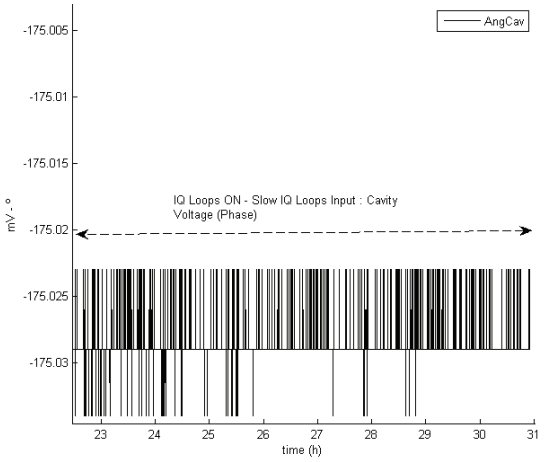

Figure 3: Long Term stability of Phase Loop.

Tuning Loop and Landau Tuning

To keep the resonance frequency of the cavity, a tuning loop compares the phase of the Forward Power of the cavity and the Cavity Voltage. In case the phase difference is outside a certain margin defined by the user (tuning dead-band), a plunger is pressed inwards/towards the cavity walls.

The landau tuning checks the amplitude of the landau cavity voltage. If it reaches a minimum value, then the plunger is moved inwards/towards the cavity walls to keep the voltage at the required level.

Automatic Start-up

In order to make easier and faster the recovery of a RF plant, an automatic start-up process was implemented in the LLRF. In standby state, the LLRF sets the RF Drive to a minimum value defined by the user and it disables all loops until RF power is detected. Once the Tx is ready and delivering power, the LLRF tunes the cavity and after that, the Amplitude and Phase loops are enabled. In the last stage of the automatic start-up the LLRF increases smoothly the RF Drive from low to nominal power. When this is achieved, the LLRF informs the operator the system is ready to start operation with beam.

Automatic Conditioning

To speed up the conditioning process of the cavities, an automatic conditioning utility was implemented: For doing this, two digital outputs of a Vacuum Gage Controller (VGC) were connected to the GPIO bus of the LLRF. These outputs are dry contacts that get opened when the vacuum pressure of the cavity is above certain limits. When the vacuum is below both pressure levels, the automatic conditioning allows increasing the RF power. If the vacuum level is above the second or higher pressure limit, the RF drive remains constant until the vacuum is again below the first or lower threshold level.

Besides this, if required, the RF Drive can also be square modulated at 10Hz. The user can adjust the duty cycle of the modulation and the amplitude at the top and bottom of the square pulse.

Fast Interlocks and Fast Data Logger

The FPGA Diagnostics Board is used to monitor mainly interlock signals, which can be reverse power at the different points of the RF plant (cavity, circulator input and output and amplifiers outputs) or other signals like Machine Protection System, Vacuum interlocks, End Switches of motor plungers and Transmitter interlocks. Whenever the reverse power at any of these points reaches a threshold defined by the user or any other interlock is detected, the Diagnostics Board will open the pin diode switches connected to the RF Drives. Besides this, it will also inform the Loops Board to set the system in standby state (loops disable and DACs input set to minimum values), the PLC controlling the RF amplifier and the general timing system.

When an interlock is detected the Diagnostics board will also trigger the Fast Data Logger (FDL). This utility consists of a 1GB RAM continuously acquiring data in a circular buffer. When a trigger is raised either on demand or due to an interlock, the acquisition is stopped and the RAM data is sent through the uTCA backplane to the host PC for post-mortem analysis.

CONCLUSIONS

The DLLRF of Max-IV based on commercial uTCA FPGA boards was assembled and commissioned with beam in 2013. The flexibility and modularity of the system has allowed adding extra features to the LLRF that have made easier the operation of the RF systems.

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